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Phone: +1 646 783 7100 | Fax: +1 646 783 7161 | customerservice@law360.com

The Challenge Of Proof In A Semiconductor Patent Case

Law360, New York (June 24, 2011) -- Microprocessor visionary Gordon Moore predicted in the 1960s that the number of transistors that could fit into a single integrated circuit would double approximately every two years. This prediction was popularly termed “Moore’s law,” and it has held true not only for transistor count, but for memory capacity and microprocessor speed as well.

Today, Moore’s Law has proven to be so accurate that it both drives competition and serves as the foundation of every long-term planning strategy and every research and development effort in the semiconductor industry. It is both a technological phenomenon and a concrete goal for some of the most brilliant engineers in Silicon Valley, Asia and elsewhere, who must constantly ask themselves: How do we make our device half as big? How do we make it twice as fast? And how can it consume less power?

The progression of Moore’s Law has been fueled by the continued shrinking of the building blocks that make up integrated circuits. In 1970, functional transistor gates were about 14 micrometers — roughly one-fourth of the width of a human hair. Today, more than 40 years later, transistor gates are measured not in micrometers, but in nanometers. To put this into scale, consider that the human fingernail grows at a rate of one nanometer per second. This means that a fingernail grows the length of two modern transistor gates, which are 30 nanometers, every minute.

Within the next decade, traditional silicon structures will reach their physical and atomic limits, and Moore’s Law will force innovations beyond transistor dimensions and process scaling techniques. Researchers are exploring the use of alternative materials to construct logic devices that will withstand continued scaling.

One such material is graphene, a type of carbon that forms honeycomb-like layers with a thickness of only one atom and exhibits electrical qualities that make it a potential replacement for silicon. Concurrent with this innovation, the U.S. Patent and Trademark Office has issued more patents for semiconductor-related technologies than any other technology class between 2006 and 2010. This includes 25,000 patents for semiconductor device manufacturing processes, 25,000 more for active solid-state devices (such as transistors), over 8,000 for computer memory, over 3,000 for digital logic circuitry, and over 2,000 for processing architectures.

Litigation inevitably occurs over such inventions, and when it does, attorneys and their testifying experts on both sides of the battle must decide very early how they will show infringement or noninfringement of the patent claims in question. This frequently means that they must show either the occurrence or existence of something that is so small as to be totally invisible to the naked eye.

This challenge is experienced by the plaintiff and defense bar alike. Plaintiffs in patent litigation must painstakingly analyze and show the operation of the defendant's device, frequently on as small as a nanoscale level, to drive settlement or prevail at trial. Defendants, on the other hand, must both analyze their own devices to refute the plaintiff's claims and sometimes analyze prior art references to the same degree.

Patent case law is far from clear about what exactly must be done to carry the burden of proving by a preponderance of evidence that a device has infringed a patent claim. In the context of conducting a pre-suit analysis to avoid filing a frivolous lawsuit under Rule 11 of the Federal Rules of Civil Procedure, courts have held that there is no per se requirement to obtain a sample or reverse engineer a defendant's product. See, e.g., Intamin Ltd. v. Magnetar Techs. Corp., 483 F.3d 1328, 1337 (Fed. Cir. 2007).

This especially makes sense in the context of modern semiconductors or integrated circuits, which likely would be either impossible to fully reverse-engineer or would force the plaintiff to incur tens of thousands of dollars or possibly more, just to file a complaint. While the requirements for avoiding frivolity under Rule 11 differ by jurisdiction, most hold that the plaintiff perform a "reasonable" investigation. The Federal Circuit has held that this means that "at a minimum, an attorney interpret the asserted patent claims and compare the accused device with those claims before filing a claim alleging infringement." Q-Pharma Inc. v. Andrew Jergens Corp., 360 F.3d 1295, 1299 (Fed. Cir. 2004).

Fortunately, for both plaintiffs and defendants, designing and building a nanoscale device such as a microprocessor or memory chip results in an enormous amount of data from various steps in the design process. This data comes in many forms, and if there is a cardinal rule in deciding which should be explored as potential evidence of infringement, noninfringement, validity or otherwise, it is that no one type of proof in semiconductor patent cases necessarily trumps all others.

Which evidence is most applicable to your case will depend on many factors, such as (1) whether the asserted claims are for a method or an apparatus; (2) whether the claims recite a particular arrangement of circuits or rather a circuit function that can be accomplished by any arrangement; (3) the level of abstraction within the semiconductor device to which the invention relates; (4) the availability of different kinds of proof; and (5) your expert's familiarity, capability and availability to delve into these different kinds of proof.

At one point in time, integrated circuits were actually designed and laid out by hand, on paper schematics. But because modern microprocessors are so complex, containing hundreds of millions or billions of transistors, engineers cannot design a processor by describing every aspect of its layout at the outset.

Instead, the circuit design must be taken through several layers of abstraction, starting with high-level diagrams and functional descriptions and ending with precise, computer-aided layout of logic gates on a floorplan and the creation of a mask to actually etch those gates into the substrate of a silicon wafer. Several examples of stages in the circuit design process, and how they might be useful as proof in litigation are discussed herein.

Levels of Circuit Design Abstraction

Paper Diagrams

Perhaps the highest level of abstraction for any logic device, be it a memory chip, digital signal processor or complex microprocessor, consists of readable diagrams found in datasheets, manuals or other high-level materials. These diagrams might display the device as a series of interconnected blocks with functional descriptions of what each block is intended to do.

Such diagrams may provide "entry-level" insights into the workings of the device at issue. Unless the patent claims are written on a similarly high level, such diagrams will not be more useful than as guidelines into further investigation or discovery.

RTL Source Code

One of the next highest levels of abstraction in the modern microprocessor is "register transfer level" or "RTL" source code, written in any number of hardware description languages (HDL). RTL code describes the operation of an integrated circuit as a series of instructions that resembles object-oriented programming languages such as C++ and Java. Particular logical operations in the RTL code are manifested later as corresponding structures, such as multiplexers, depending on later decisions by both the designer and automated tools.

RTL code is just one of many forms of data that often dictate the design of a microprocessor, and it may be useful evidence if the patent claims at issue recite an integrated circuit, at a relatively high level, that performs a certain function through any number of different physical layouts. In contrast, RTL code may not be as useful if the patent claims recite a very particular layout of logic gates within the circuit, because RTL code, by itself, may not dictate exactly which gates go where.

Netlists

Advancing the integrated circuit design from the RTL stage to physical circuitry produces yet more data that might be useful in patent litigation. This process is typically called "logic synthesis" and today is achieved with heavy reliance on software suites from vendors such as Synopsys Inc. and Cadence Inc. The process and software used can vary depending on the complexity of the intended final circuit.

Given guidance, this type of software makes decisions on what kind and how many logic gates should be used to achieve the higher-level goal of the RTL code, and the output of this process is often a file referred to as a "netlist" or "gate-level netlist." These files are other potentially valuable means by which a technical expert can show the presence or absence of structure described in a precise manner, because netlists can indicate the intended presence or absence of specific logic structures and gates.

GDS Layouts

Yet another major stage in the circuit design process is the shift from a netlist to an actual layout that can be used by the chip fabricator to make the chip. Again, software is used to translate the netlist into a file that will describe exactly how the chip will be physically implemented. These files are typically called GDS ("Graphic Database System") layouts, and they describe precisely which logic gates and buses are located on multiple layers of the device, and how those layers are interconnected.

GDS layouts can be mined with viewing tools to locate structure exactly as it should appear in the physical device. As such, GDS layouts represent one of the lowest level forms of proof that might be available to attorneys and their testifying experts. If the patent claims at issue describe low-level features that must be in a particular order or sequence to carry out the invention, then GDS layouts might be the best available proof.

RTL source code, netlists, GDS layouts, and other similar data not specifically mentioned, share a common trait in that they are ways of describing what the eventual integrated circuit should do and should look like. These files, collectively, often represent a blueprint for thousands or millions of individual devices before they are physically implemented.

Therefore, using these data sources as a means for your testifying expert to show the presence or absence of structure reading on particular patent claim elements will naturally move infringement proof from direct to circumstantial because the accused device is not being observed directly.

This is not a problem, as the Federal Circuit has expressly and repeatedly recognized that circumstantial evidence can be credible and persuasive in proving infringement. See, e.g., Moleculon Research Corp. v. CBS Inc., 793 F.2d 1261 (Fed. Cir. 1986) ("[I]t is hornbook law that direct evidence of a fact is not necessary. Circumstantial evidence is not only sufficient, but may also be more certain, satisfying and persuasive than direct evidence.") (quoted in Lucent Techs. Inc. v. Gateway Inc., 580 F.3d 1301, 1318 (Fed. Cir. 2009)); see also Alco Std. Corp. v. Tenn. Valley Auth., 808 F.2d 1490, 1503 (Fed. Cir. 1986) ("Although the evidence of infringement is circumstantial, that does not make it any less credible or persuasive.")

As with any litigation strategy, attention must be paid to not only "hornbook law," but the persuasive impact of the potentially proffered evidence. To this end, it may be advantageous to go beyond circumstantial evidence. There are means of showing the presence or absence of structure by direct observation through extremely advanced and powerful techniques for cutting open a device and looking at it under a microscope. This is typically called a "teardown," and can be done effectively through a handful of experienced firms.

Teardowns can be done at several different levels of microscopy, and at the lowest level can even detect physical structures not much larger than a few molecules. Further, for some semiconductor patent claims, which read on a particular transistor, capacitor or other fundamental structure, a teardown may be critical proof that is not otherwise available in the electronic forms described above.

Teardowns, however, are quite expensive. The need for one, which can run into the hundreds of thousands of dollars in cost, should be factored in very early in the process of either pursuing or defending against patent infringement claims.

Even when several or all of the different types of data described above are available, other proof problems may arise in a patent infringement case involving integrated circuits. Though the electronic evidence might show clearly that the circuit design shows X and the teardown of a finished device shows Y, attorneys must still connect the dots between this evidence and their royalty base.

One cannot assume that a given RTL routine or GDS layout actually resulted in the structure photographed at your teardown. Even if it does, one cannot assume that every one of the defendant's millions of other devices were designed or built in the same way.

This presents tremendous opportunities for creative lawyering and potential collaboration between opposing sides. It may be possible, for example, for opposing sides to agree that because the operation of one device is so likely to be similar to other devices, or that electronic materials describing one device are likely to describe all other devices at issue, that establishing exemplars would greatly decrease discovery and other litigation costs. See, e.g., TiVo Inc. v. EchoStar Comm'ns Corp., 516 F.3d 1290, 1308 (Fed. Cir. 2008) ("[T]here is nothing improper about an expert testifying in detail about a particular device and then stating that the same analysis applies to other allegedly infringing devices that operate similarly, without discussing each type of device in detail.") Such cooperation is sure to benefit judge, jury, clients, attorneys and experts alike.

Mapping patent claim elements to modern integrated circuits and semiconductor devices is a complicated process, and care must be taken to ensure that your expert is receiving the right data for the claims at issue. In the end, there are several ways to carry the burden of proving infringement or, from a defendant's perspective, putting forth a compelling noninfringement case.

While the considerations above are by no means exhaustive, taking them into account early in the case and undergoing the appropriate preparations will go a long way toward a successful result.

--By Anthony G. Beasley, William H. Manning, Jacob S. Zimmerman, Aaron R. Fahrenkrog and Samuel L. Walling, Robins Kaplan Miller & Ciresi LLP

Anthony Beasley, Jacob Zimmerman, Aaron Fahrenkrog and Samuel Walling are intellectual property litigation associates in the Minneapolis office of Robins Kaplan Miller & Ciresi. William Manning is a partner in the firm's Minneapolis office.